(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 476 625 B1

# (12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
**23.07.1997 Bulletin 1997/30**

(51) Int Cl.[6]: **H01L 21/3205**, H01L 21/768, H01L 23/482, H01L 23/522

(21) Application number: **91115858.2**

(22) Date of filing: **18.09.1991**

## (54) A process of producing a semiconductor device having multilevel interconnections

Verfahren zum Herstellen einer Halbleiteranordnung mit Mehrlagen-Verbindungsleitungen

Procédé de fabrication d'un dispositif semi-conducteur ayant des interconnexions multicouches

(84) Designated Contracting States:
**DE FR GB**

(30) Priority: **18.09.1990 JP 248235/90**

(43) Date of publication of application:
**25.03.1992 Bulletin 1992/13**

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(56) References cited:
**EP-A- 0 373 360** **EP-A- 0 393 635**
**US-A- 4 920 639**

- **IBM TECHNICAL DISCLOSURE BULLETIN. vol. 32, no. 8A, January 1990, NEW YORK US pages 88 - 89; 'structure and method for making multilayer air bridge wiring'**
- **pages 88 - 89; 'structure and method for making multilayer air bridge wiring'**
- **PATENT ABSTRACTS OF JAPAN vol. 3, no. 207 (E-758)16 May 1989 & JP-A-1 024 444 ( FUJITSU ) 26 January 1989**



EP 0 476 625 B1

## Description

The present invention relates to a process of producing a semiconductor device having multilevel interconnections.

In recent years, the integration density of semiconductor devices has been raised and multilevel interconnections have been used more frequently, as the scale of the systems realized by the use of semiconductor devices is increased and the fabrication technology for semiconductor devices with fine geometry is advanced.

With the increase in the integration density of semiconductor devices, the space between the interconnections also decreases. Because of this, the parasitic capacitance incidental to the interconnections increases.

In order to reduce such parasitic capacitance, it has been proposed to remove an inter-layer insulation film to make the space between the interconnection layers vacant, by supporting the upper layer interconnection only by contact pillars at via hole positions, in a report by Eiichi YAMAMOTO, et al. entitled "Multilevel Metal Interconnect for Ultra High Speed LSI using Al/Polymide Contact Pillar Method" numbered 456 in a preprint article of "Electronic Information Communication Society 70th Anniversary General National Grand Meeting" (1987) at pages 2-260. In such multilevel interconnections of aerial interconnection construction as above, the coupling capacitance between interconnection levels is reduced to 1/4 to 1/3 of that of ordinary multilevel interconnections completely filled with inter-layer insulating films.

The above-mentioned prior art multi-level interconnections having aerial interconnection construction is considered to have ideal construction with respect to reduction of coupling capacitance between interconnection levels, but to have a defect that it is weak against mechanical impact since the physical support between interconnection levels is achieved only by conductive contact pillars for electrically connecting interconnection levels. Further, thermal stress of interconnections caused by thermal expansion owing to Joule's heat is not dispersed but concentrated to the contact pillars. For such thermal and mechanical impacts, it is liable to occur that interconnections are cut open or short-circuited and so it is impracticable to really apply the multilevel interconnections having aerial interconnection construction to a large scale integrated circuit.

The present inventor formerly presented together with other co-inventors, in EP-A-0 393 635 [corresponding to Japanese Patent Application No. 104,967/1990 filed on April 20, 1990] a semiconductor device that has a feature in the spatial relationship between interconnection levels and the intermediate insulating films. In the lower part of the second and/or subsequent levels of interconnection there exist intermediate insulating films that have a pattern which is the same as the pattern of the interconnection. Because of this arrangement, the intermediate insulating film does not exist between the interconnections on the same level. The first structure of the multilevel interconnection has the intermediate insulating films formed in wall-like shape, with the lower end of the intermediate insulating films reaching an underlying insulating layer formed on the surface of the semiconductor substrate. The second structure of the multilevel interconnection is a quasi air gap metallization structure. This construction has markedly improved thermal and mechanical strength compared with the above-mentioned aerial interconnection construction, but the reduction of coupling capacitance between interconnection levels is not so large as the aerial interconnection construction.

In a semiconductor device known from EP-A-0 373 360 spaces are formed between the lower-level interconnections which spaces are sealed by the substrate and by an upper level insulating layer, wherein the spaces are filled by an inert gas with low pressure which gives a low dielectric constant. Furthermore, this document discloses method steps 1) to 7) of the appended claim.

An aerial interconnection construction as described before is disclosed in US-A-4 920 639.

It is an object of the invention to provide process of producing a semiconductor device which obtains both the reduction of coupling capacitance between interconnection levels and improvement of thermal and mechanical strength.

This object is achieved by a method for the production of a semiconductor device as defined in the appended claim.

Fig. 1 shows a perspective view to schematically explain the structure of a semiconductor device to be produced.

Figs. 2(a) to 2(h) and Figs. 3(a) to 3(e) show cross sections to schematically explain the production steps of a semiconductor device as an embodiment of the present invention.

Figs. 4(a) to 4(h) and Figs 5(a) to 5(1) show cross sections to schematically explain an extension of the production steps of a semiconductor device.

The present invention will be explained below further in detail with respect to its some embodiments shown in Figs. 1 to 5.

In Fig. 1, an example of two-level interconnections is shown by a perspective view, wherein on a lower level inorganic insulating film 1 consisting for instance of a silicon oxide film formed on a semiconductor substrate 20, first-level interconnections 2 consisting for instance of aluminium are formed. The space between the first-level interconnections 2 is vacant to form a cavity. On the first-level interconnections 2, second-level interconnections 6 consisting of aluminium or the like are formed with interposed first inter-level inorganic insulating film 3 consisting for instance of a silicon oxide film. The first inter-level inorganic insulating film 3 exists at solid crossing points between the first-level interconnections 2 and the second-level interconnections 6, excepting via

hole portions (not shown in the drawing) for forming contact pillars which electrically connect the first-level interconnections 2 and the second-level interconnections 6. Further, the first-level inorganic insulating film 3 does not exist at portions other than the above mentioned crossing points and so these portions are vacant to form a cavity.

In this device, the first-level and the second-level interconnections form solid crossing points with an interposed inter-level inorganic insulating film at portions other than via hole portions, differently from the above mentioned aerial interconnection construction. Therefore the second-level interconnections 6 are mechanically supported on the first-level interconnections 2 also at these solid crossing points. It can be considered that this construction has the same construction as the ordinary multilevel interconnections wherein the space between interconnections is fully filled with an inter-level insulating film only at the above mentioned solid crossing points, and the same construction as the aerial interconnection construction at the other portions. Since the ratio of the above mentioned solid crossing points occupied in the entire coupling capacitance is ordinarily not higher than 1/4, although it depends upon configuration of interconnections, it can be said that the coupling capacitance in this device is only 1/3 to 1/4 of that of the ordinary multilevel interconnections wherein the space between interconnections is fully filled with an inter-level insulating film.

Next, an embodiment of the present invention will be explained with reference to Figs. 2(a) to 2(h) which are cross sections along the line A-A' in Fig. 1 in the direction of the second-level interconnections 6 and Figs. 3(a) to 3(e) which are cross sections along the line B-B' in Fig. 1 in the direction of the first-level interconnections 2.

First, as shown in Fig. 2(a), a lower level inorganic insulating film 1 for instance of silicon oxide is formed on a semiconductor substrate 20 and a first-level interconnection layer for instance of aluminium is formed to have a thickness of about 0.5 μm. Further, a first inter-level inorganic insulating film 3 for instance of silicon oxide is formed thereon to have a thickness of about 0.5 μm. Next, a photoresist is coated and patterned, the first inter-level inorganic insulating film 3 and the first-level interconnection layer are etched by using the patterned photoresist as a mask to form first-level interconnections 2, and the photoresist is removed. Next, as shown in Fig. 2(b), a first inter-level organic insulating film 4 is formed to have a thickness of about 1.5 μm by polyimide by means of a spin-on method.

Then as shown in Fig. 2(c), the first inter-level organic insulating film 4 is etched by a plasma etching method by using oxygen gas, so that the surface of the first inter-level inorganic insulating film 3 is exposed but the first inter-level organic insulating film 4 existing at lateral side of the first inter-level inorganic insulating film 3 is retained. Next as shown in Fig. 2(d), via holes 5 are opened at desired positions in the first inter-level inorganic insulating film 3 by means of an ordinary photolithography method.

Then as shown in Fig. 2(e), a second-level interconnection layer 6A is formed to have a thickness of about 0.5 μm by an aluminium film by means of a magnetron sputtering method. Next, as shown in Figs. 2(f) and 3 (a), a photoresist is coated and patterned to form a mask 7 for second-level interconnections.

As shown in Fig. 3(b), the second-level interconnection layer 6A is patterned by anisotropic plasma etching by a chlorine-containing gas through the mask 7 to form the second-level interconnections 6. Next as shown in Fig. 3(c), the first inter-level inorganic insulating film 3 is patterned by anisotropic plasma etching by a fluorine-containing gas.

The mask 7 is then removed as shown in Figs. 2(g) and 3(d). The first inter-level organic insulating film 4 is removed as shown in Figs. 2(h) and 3(e) by isotropic plasma etching by oxygen gas to form a cavity 8. This can be carried out simultaneously with removal of the mask 7 in the former production step.

By this embodiment of the present invention, it is possible to realize the interconnection construction as shown in Fig. 1. In this production process, it is possible to make the patterning of the first inter-level inorganic insulating film 3 by utilizing the lithography of the patterning of the first-level interconnections 2 and that of the second-level interconnections 6 and so no additional lithography steps are required. This enables to avoid increase of number of production steps.

Fig. 4(a) to 4(h) and 5(a) to 5(l) show an extension of the process wherein third-level interconnections are formed in addition to the two-level interconnection construction as shown in the above mentioned embodiment. The third-level interconnections are formed along the line B-B' in Fig. 1 in the direction of the first-level interconnections 2. Figs. 4(a) to 4(h) are cross sections along the line A-A' in Fig. 1 in the direction of the second-level interconnections 6 and Figs. 5(a) to 5(l) are cross sections along the line B-B', in Fig. 1 in the direction of the first-level interconnections 2.

As shown in Figs. 4(a) and 5(a), the construction as shown in Fig. 2(e) of the embodiment of the present invention is formed, that is, up to the formation of the second-level interconnection layer 6A. Then a second inter-level inorganic insulating film 9 for instance of silicon oxide is formed thereon to have a thickness of about 0.5 μm. Next, the photoresist for the second-level interconnections is patterned to form a mask 10. As shown in Fig. 5(b), the second inter-level inorganic insulating film 9 is patterned by anisotropic plasma etching by a fluorine-containing gas through the mask 10.

As shown in Fig. 5(c), the second-level interconnection layer 6A is patterned by anisotropic plasma etching by a chlorine-containing gas to form the second-level interconnections 6. Then as shown in Fig. 5(d), the first inter-level inorganic insulating film 3 is patterned by an-

isotropic plasma etching by a fluorine-containing gas.

As shown in Figs. 4(b) and 5(e), the mask 10 is removed and as shown in Figs. 4(c) and 5(f), a second inter-level organic insulating film 11 is formed to have a thickness of about 2 μm by polyimide by means of a spin-on method.

Then as shown in Fig. 5(g), the second inter-level organic insulating film 11 is etched by a plasma etching method by using oxygen gas, so that the surface of the second inter-level inorganic insulating film 9 is exposed but the second inter-level organic insulating film 11 existing at lateral side of the second inter-level inorganic insulating film 9 is retained. Next as shown in Fig. 5(h), via holes 12 are opened at desired positions in the second inter-level inorganic insulating film 9 by means of an ordinary photolithography method.

Then as shown in Fig. 5(i), a third-level interconnection layer 13A is formed to have a thickness of about 0.5 μm by an aluminium film by means of a magnetron sputtering method. Next, as shown in Figs. 4(d) and 5(j), a photoresist is coated and patterned to form a mask 14 for a third-level interconnections.

As shown in Fig. 4(e), the third-level interconnection layer 13A is patterned by anisotropic plasma etching by a chlorine-containing gas through the mask 14 to form the third-level interconnections 13. Next as shown in Fig. 4(f), the second inter-level inorganic insulating film 9 is patterned by anisotropic plasma etching by a fluorine-containing gas.

The mask 14 is then removed as shown in Figs. 4 (g) and 5(k). The first inter-level organic insulating film 4 and the second inter-level organic insulating film 11 are removed as shown in Figs. 4(h) and 5(l) by isotropic plasma etching by oxygen gas to form a cavity 15 and a cavity 16. This can be carried out simultaneously with removal of the mask 14 in the former production step.

In this process, it is possible to make the patterning of the first inter-level inorganic insulating film 3 by utilizing the lithography of the patterning of the first-level interconnections 2 and that of the second-level interconnections 6 and also to make the patterning of the second inter-level inorganic insulating film 9 by utilizing the lithography of the patterning of the second-level interconnections 6 and that of the third-level interconnections 13 and so no additional lithography steps are required. This avoids, an increase of the number of production steps.

The interconnection construction as formed has small coupling capacity owing to shall dielectric constant of the cavities. Further, since the second-level interconnections 6 are supported by the first inter-level inorganic insulating film 3 and the third-level interconnections 13 are supported by the second inter-level inorganic insulating film 9, a three-level interconnection construction durable against thermal and mechanical impacts can be obtained.

As explained above in detail, an inter-level insulating film is formed at solid crossing points between upper-level interconnections and lower-level interconnections, excepting via hole portions. This means that mechanical support between interconnection levels is given by solid crossing points between interconnections. For this, a semiconductor device having high durability against thermal and mechanical impacts can be obtained.

Further, since inter-level regions other than the solid crossing points are made vacant to form a cavity, coupling capacity can be reduced to 1/3 to 1/4 of an ordinary multilevel interconnections wherein inter-level regions are fully filled with an inter-level insulating film.

## Claims

1. A process of producing a semiconductor device having multilevel interconnections, the process comprising the following steps :

   1) forming on a semiconductor substrate (20), a lower-level inter-level insulating film (1) of an inorganic material,
   2) forming on the lower-level inter-level insulating film (1), a lower-level interconnection layer, an upper-level inter-level insulating film (3) of an inorganic material and a photoresist film in this order,
   3) patterning the photoresist film to form a first mask,
   4) patterning by means of this first mask, the upper-level inter-level insulating film (3) and the lower-level interconnection layer to form lower-level interconnections (2),
   5) forming an organic insulating film (4) on the entire surface including the patterned upper-level inter-level insulating film (3) and filling the spaces therebetween after removing the first mask,
   6) etching the organic insulating film (4) to expose the surface of the patterned upper-level inter-level insulating film, wherein the organic insulating film (4) remains in said spaces,
   7) forming via holes (5) in the exposed upper-level inter-level insulating film,
   8) forming an upper level interconnection layer (6A) on the entire surface and at the same time filling the via holes with this upper-level interconnection layer,
   9) forming on this upper-level interconnection layer a photoresist film and patterning the same to form a second mask (7),
   10) patterning by means of this second mask, the upper-level interconnection layer (6A) and the upper-level inter-level insulating film (3) to form upper-level interconnections (6) having crossing points with the lower-level interconnections (2), said upper-level inter-level insulating film (3) remaining at the crossing points

thus forming solid crossing points, and
11) selectively removing the second mask (7) and the remaining organic insulating film (4) to form a cavity (8, 15, 16) between the lower-level insulating film (1) and the upper level interconnections (6).

zungspunkte gebildet werden, und
11) selektives Entfernen der zweiten Maske (7) und des verbleibenden organischen Isolierfilms (4) zur Ausbildung eines Hohlraums (8, 15, 16) zwischen dem Unterlagenisolierfilm (1) und den Oberlagen-Verbindungen (6).

**Patentansprüche**

1. Verfahren der Herstellung einer Halbleitervorrichtung mit Mehrlagenverbindungen, wobei der Prozeß die folgenden Schritte aufweist:

   1) Ausbilden eines Unterlagen-Zwischenlagen-Isolierfilms (1) aus anorganischem Material auf einem Halbleitersubstrat (20),
   2) Ausbilden einer Unterlagen-Verbindungsschicht, eines Oberlagen-Zwischenlagen-Isolierfilms (3) aus einem anorganischen Material und eines Fotoresist-Films in dieser Reihenfolge auf dem Unterlagen-Zwischenlagen-Isolierfilm,
   3) Strukturieren des Fotoresist-Films zur Ausbildung einer ersten Maske,
   4) Strukturieren mittels dieser ersten Maske des Oberlagen-Zwischenlagen-Isolierfilms (3) und der Unterlagen-Verbindungsschicht zur Ausbildung von Unterlagenverbindungen (2),
   5) Ausbilden eines organischen Isolierfilms (4) auf der Gesamtoberfläche einschließlich des strukturierten Oberlagen-Zwischenlagen-Isolierfilms (3) und Ausfüllen der Räume dazwischen nach dem Entfernen der ersten Maske,
   6) Ätzen des organischen Isolierfilms (4) zum Freilegen der Oberfläche des strukturierten Oberlagen-Zwischenlagen-Isolierfilms, wobei der organische Isolierfilm (4) in den Räumen verbleibt,
   7) Ausbilden von Durchgangslöchern (5) in dem freigelegten Oberlagen-Zwischenlagen-Isolierfilm,
   8) Ausbilden einer Oberlagen-Verbindungsschicht (6A) auf der gesamten Oberfläche und gleichzeitig Ausfüllen der Durchgangslöcher mit dieser Oberlagen-Verbindungsschicht,
   9) Ausbilden eines Fotoresist-Films auf dieser Oberlagen-Verbindungsschicht und Strukturierung desselben zur Ausbildung einer zweiten Maske (7),
   10) Strukturieren der Oberlagen-Verbindungsschicht (6A) und des Oberlagen-Zwischenlagen-Isolierfilms (3) mittels dieser zweiten Maske zum Ausbilden von Oberlagen-Verbindungen (6), die Schnittpunkte mit den Unterlagenverbindungen (2) aufweisen, wobei der Oberlagen-Zwischenlagen-Isolierfilm (3) an den Schnittpunkten verbleibt, so daß feste Kreu-

**Revendications**

1. Procédé de fabrication d'un dispositif semi-conducteur ayant des interconnexions multicouches, le procédé comprenant les étapes suivantes :

   1) former sur un substrat semi-conducteur (20) un film d'isolation des niveaux du niveau inférieur (1) d'une matière minérale,
   2) former sur le film d'isolation des niveaux du niveau inférieur (1) une couche d'interconnexion du niveau inférieur, un film d'isolation des niveaux du niveau supérieur (3) d'une matière minérale et un film en résine photosensible dans cet ordre,
   3) tracer l'impression du film en résine photosensible pour former un premier masque,
   4) tracer, au moyen de ce premier masque, l'impression du film d'isolation des niveaux du niveau supérieur (3) et de la couche d'interconnexion du niveau inférieur pour former des interconnexions du niveau inférieur (2),
   5) former un film organique isolant (4) sur la surface totale comportant le film d'isolation des niveaux du niveau supérieur (3) de l'impression et remplir les espaces dans celui-ci après avoir éliminé le premier masque,
   6) graver le film organique isolant (4) pour exposer la surface du film d'isolation des niveaux du niveau supérieur de l'impression, le film organique isolant (4) restant dans lesdits espaces,
   7) former des trous traversants (5) dans le film d'isolation des niveaux du niveau supérieur exposé,
   8) former une couche d'interconnexion du niveau supérieur (6A) sur la surface totale et en même temps remplir les trous traversants de cette couche d'interconnexion du niveau supérieur,
   9) former sur cette couche d'interconnexion du niveau supérieur un film en résine photosensible et tracer l'impression de celui-ci pour former un deuxième masque (7),
   10) tracer, au moyen de ce deuxième masque, l'impression de la couche d'interconnexion du niveau supérieur (6A) et du film d'isolation des niveaux du niveau supérieur (3) pour former des interconnexions du niveau supérieur (6) ayant des points d'intersection avec les inter-

connexions du niveau inférieur (2), ledit film d'isolation des niveaux du niveau supérieur (3) restant aux points d'intersection formant donc des points d'intersection solides, et

11) éliminer sélectivement le deuxième masque (7) et le film organique isolant (4) restant pour former une cavité (8, 15, 16) entre le film isolant du niveau inférieur (1) et les interconnexions du niveau supérieur (6).

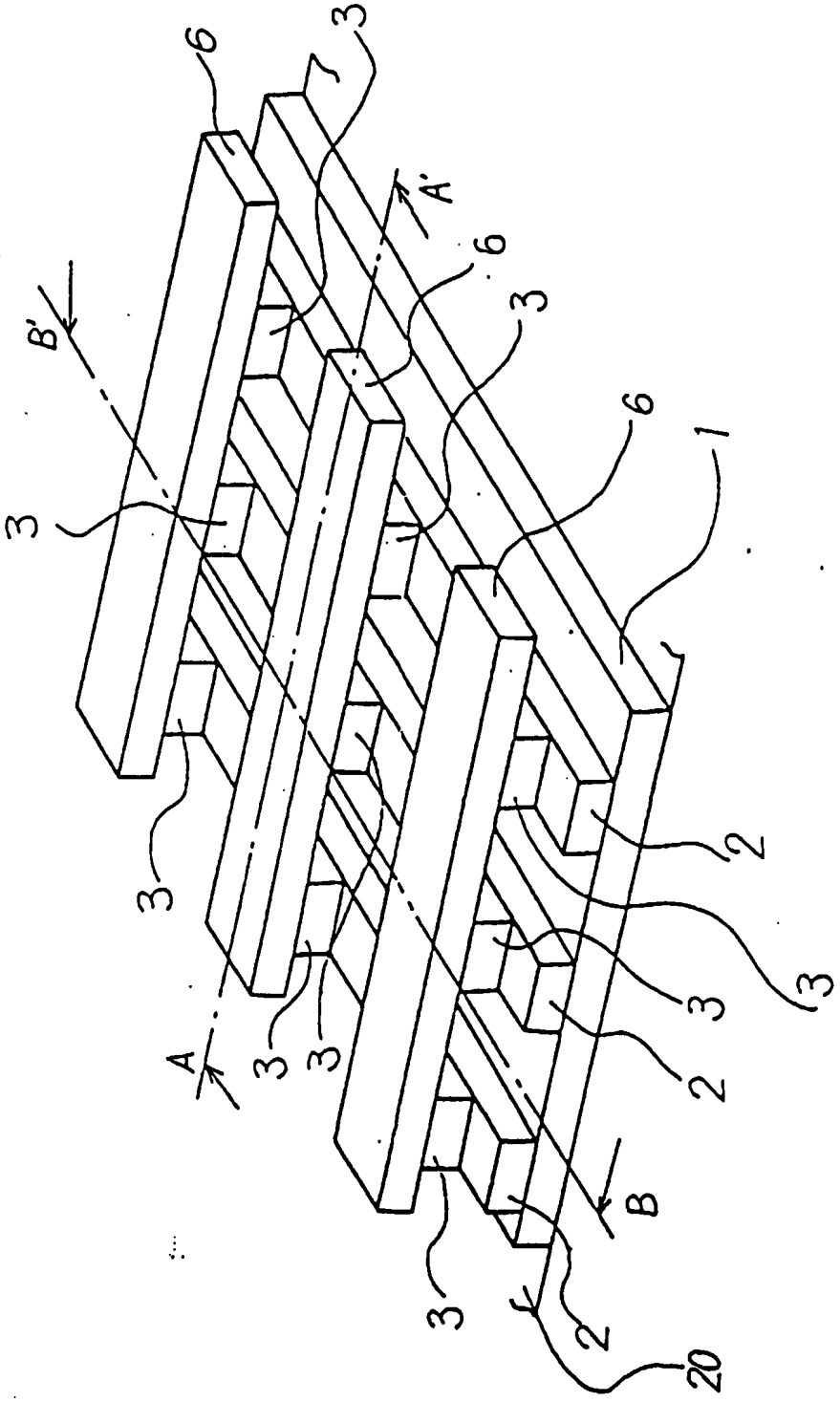



Fig. 1

Fig. 2(a)

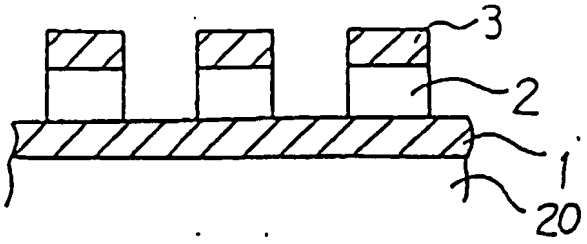



Fig. 2 (b)

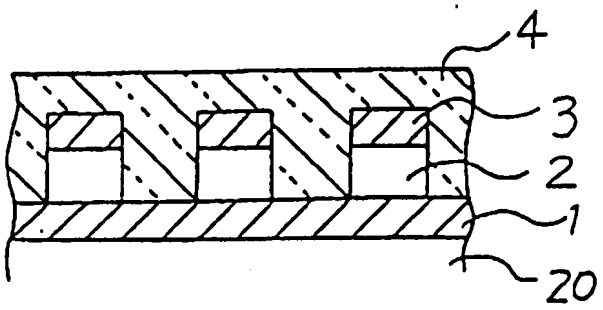



Fig. 2(C)

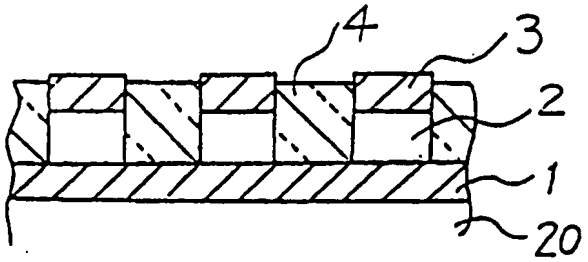



Fig. 2(d)

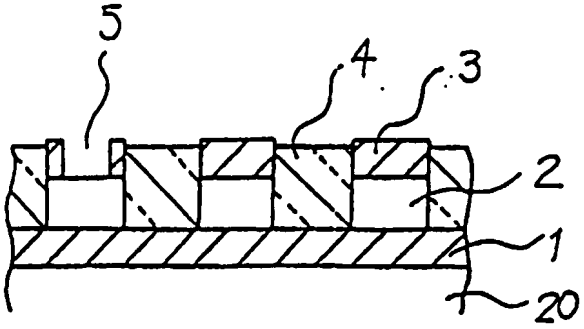


Fig. 2(e)

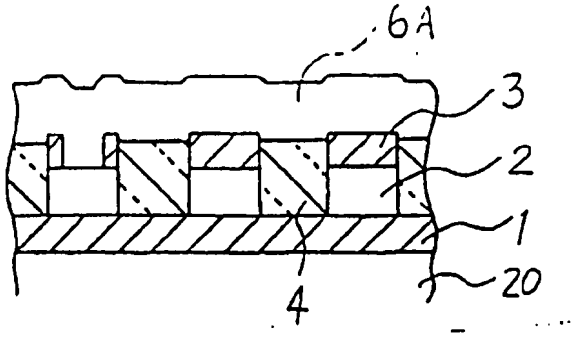



Fig. 2 (f)

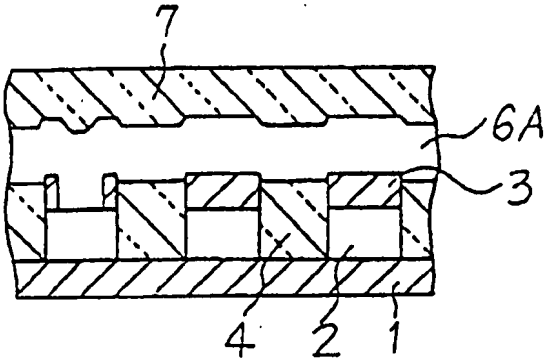



Fig. 2 (g)

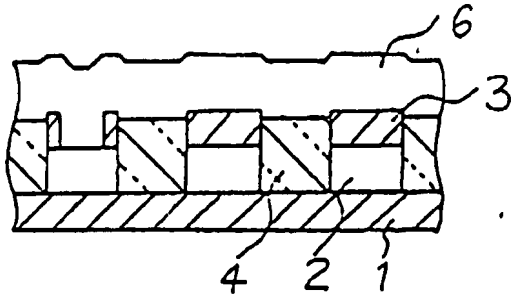



Fig. 2 (h)

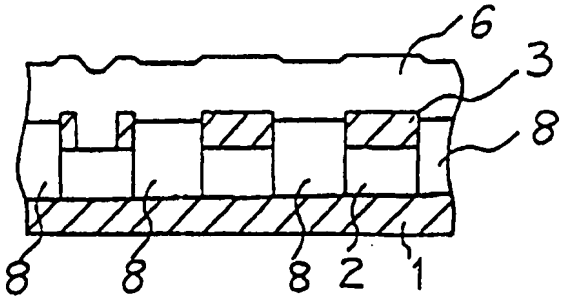


Fig. 3 (a)

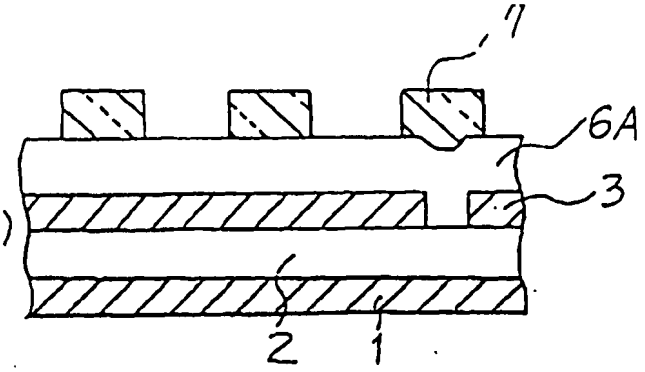



Fig. 3 (b)

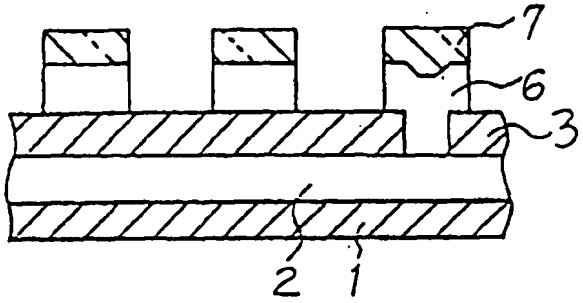



Fig. 3 (C)

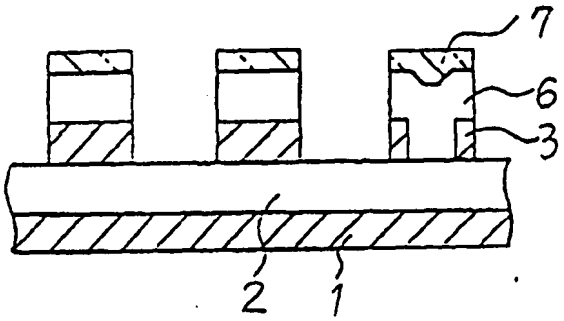



Fig. 3 (d)

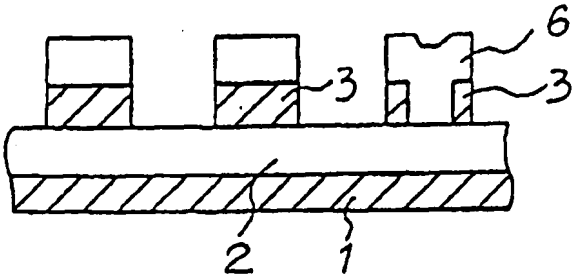
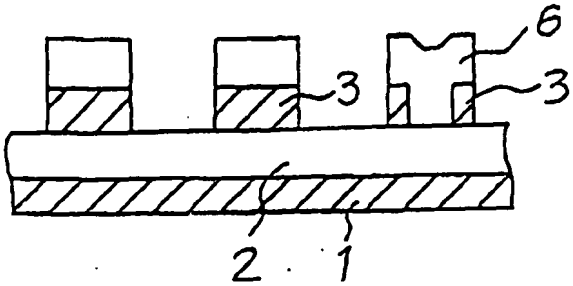



Fig. 3 (e)



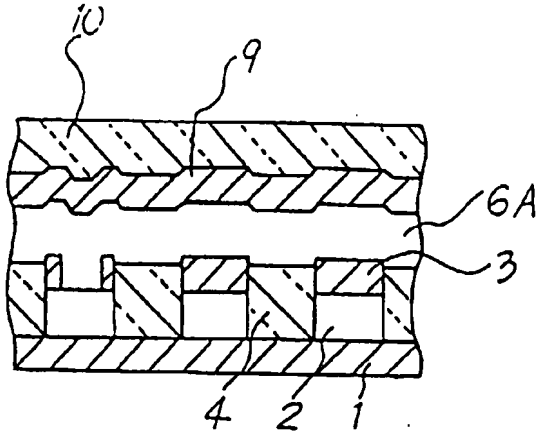



Fig. 4 (a)

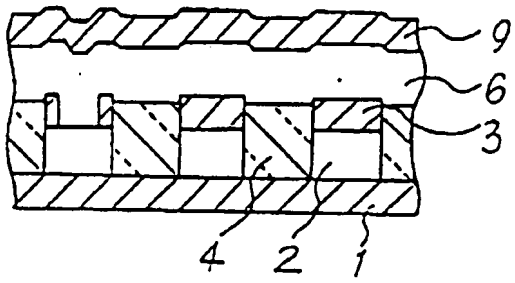



Fig. 4 (b)

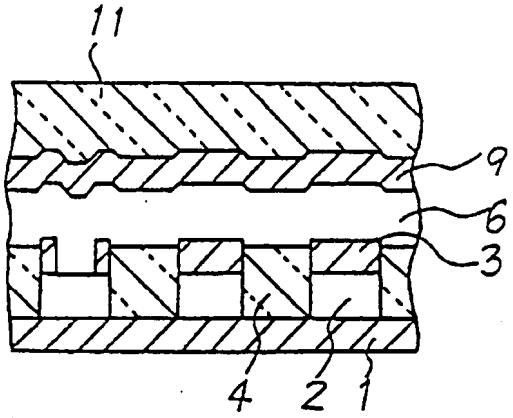



Fig. 4 (C)

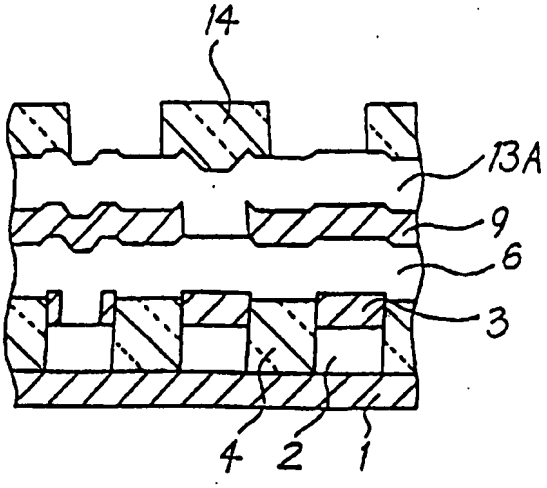



Fig. 4 (d)

Fig. 4 (e)

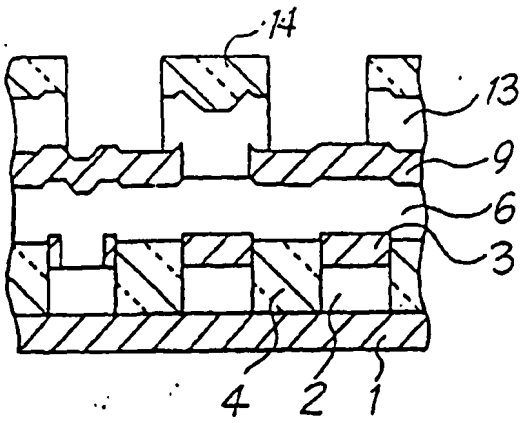



Fig. 4 (f)

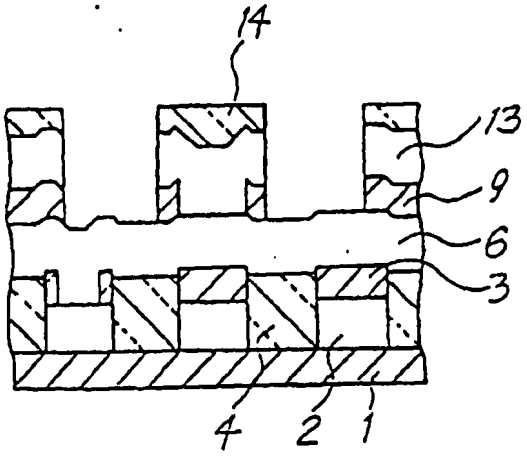



Fig. 4(g)

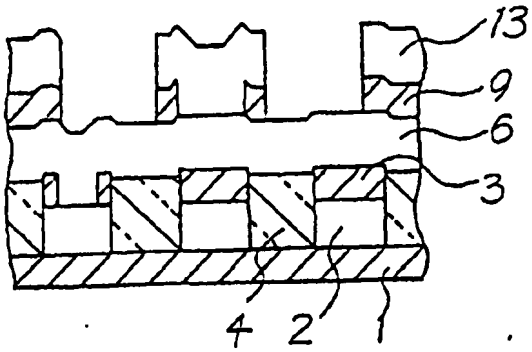



Fig. 4(h)

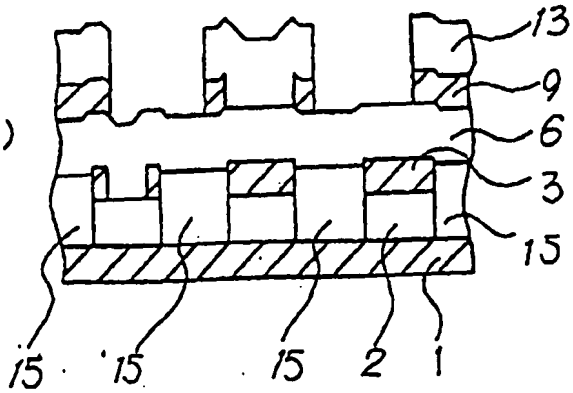


Fig. 5 (a)

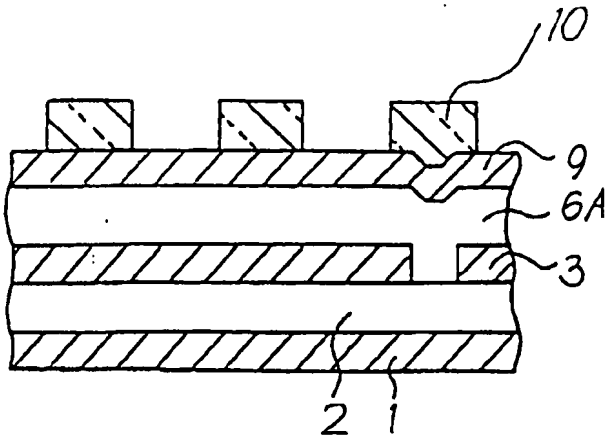



Fig. 5 (b)

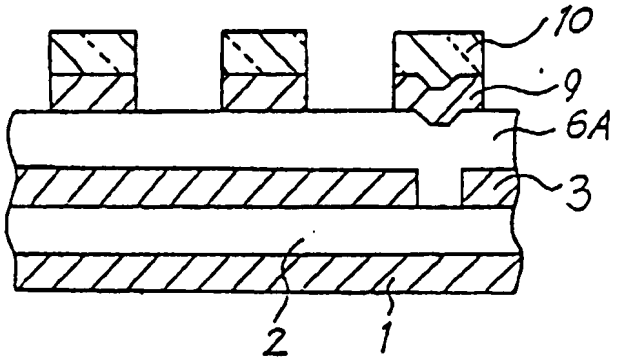



Fig. 5 (C)

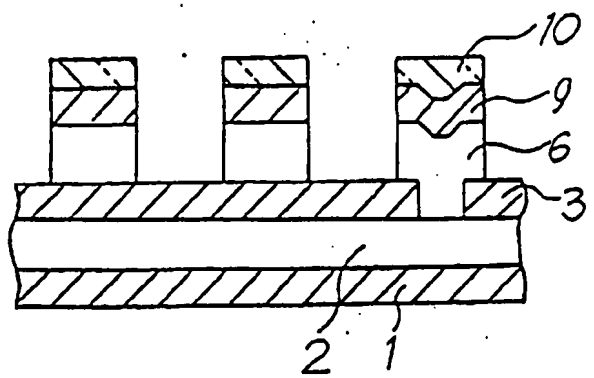



Fig. 5 (d)

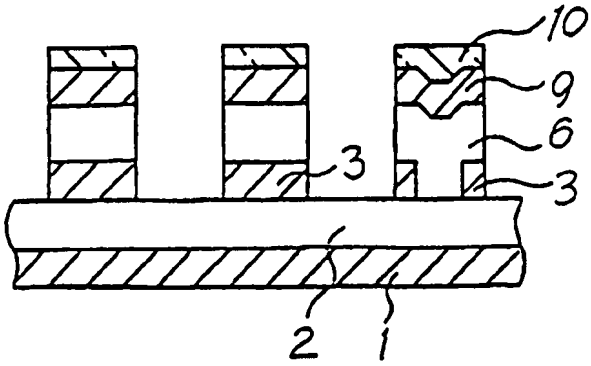


Fig. 5 (e)

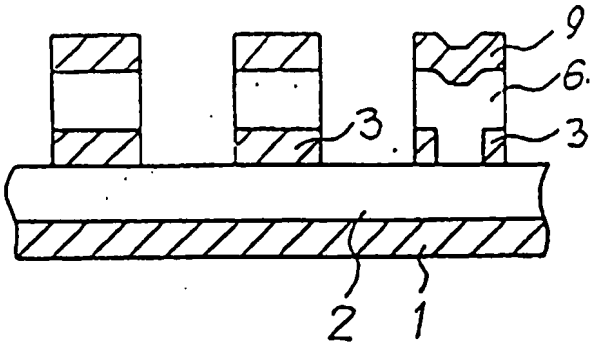



Fig. 5 (f)

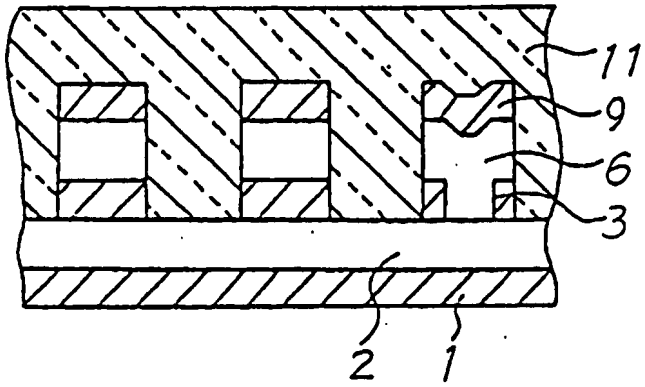



Fig. 5 (g)

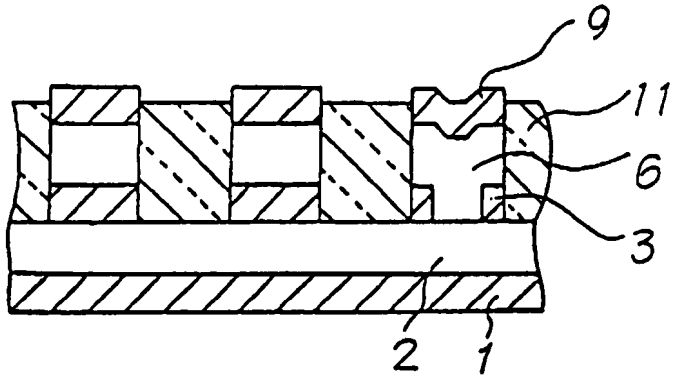



Fig. 5 (h)

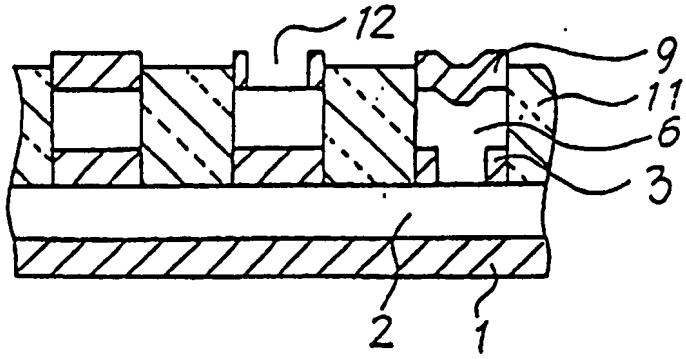


Fig. 5 (i)

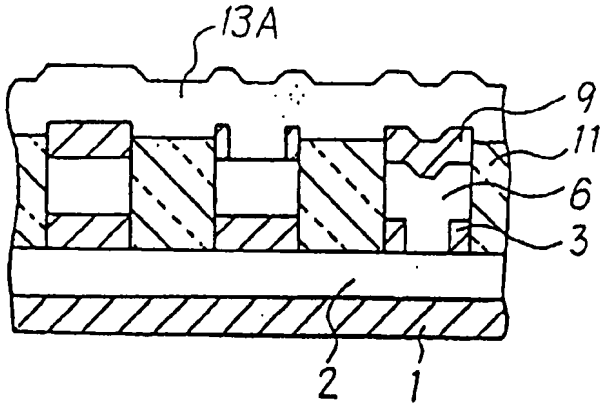



Fig. 5 (j)

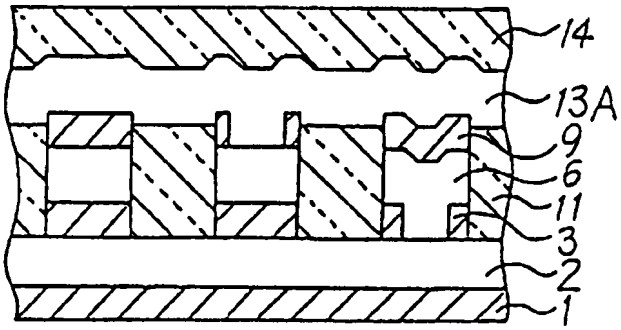



Fig. 5 (k)

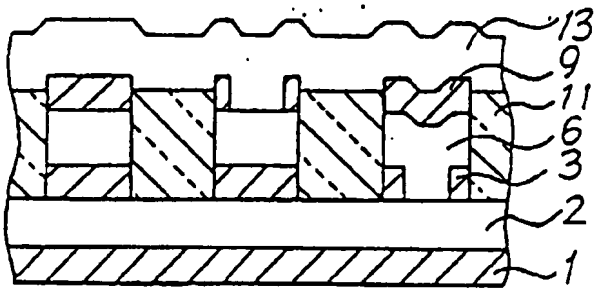



Fig. 5 (l)